ABSTRACT

Apparatus having a cache memory including cache lines configured to cache data sent from an input/output device and an eviction mechanism configured to evict data stored in one of the cache lines based on validity state information associated with the data stored in the one cache line. Each cache line has multiple portions, and validity bits are used to track the validity of respective portions of the cache line. The validity bits are set to predefined values responsive to the number of bytes written into the respective portions in one write transaction. The cache line is evicted by the eviction mechanism when the validity bits corresponding to the cache line all have the predefined values. The eviction mechanism is configured to evict the data even if the cache memory is not full.